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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,027	SNYDER, WARREN	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/30/02,04/05/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Clams 1-59 are presented for examination. This Office action is based the renumbered sequnce of the clams as amended by applicant on 04/05/02. The total claims are 1-59, not 1-60.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

See the Certificate of Correction for the PCT filing date on Dec. 30, 1996 of the 6,460,172 patent.

2. Claims 1,3-8,11-22,25-32,35-41,51-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Insenser Farre et al. (6,460,172).

3. As to claim 1, Insenser Farre et. ("Insenser" hereafter) disclosed a circuit [FIPSOC] (see fig.1) comprising at least :

a) a bus [9];

b) a microprocessor coupled to the bus (not explicitly shown in the figure, but taught in col.2, lines 40-51, col.3, lines 22-24 as on-chip microprocessor);

c) memory [1] :

a plurality of functionalities ([3][4]). Comprising

1) interconnect (see the connection to [3] and [4]);

2)analog circuit ([4]);

3) a digital functional block to the interconnect (see fig.1[3]).

4. AS to claims 3, 4, Insenser also included programmable I/O (see fig.1 [5], col.3, lines 18-19, see also col.2, lines 1-14 for background teaching of programmable logic blocks).

5. As to claims 5,6, Insenser also included analog functional block [4] and digital functional block [4] (see fig.1, col.1, lines 15-19, see also col.2, lines 1-14 for background teaching of programmable logic blocks).

6. As to claim 7, Insenser also included configuration state (see also col.2, lines 1-14 for background teaching of programmable configuring and reconfiguring features of logic blocks, see the configuration contexts in col.4, lines 1-7).

7. As to claim 8, see the CAD tools in fig.4 for user input).

8. As to claim 11,Insenser also taught :

a) a bus [9];

b) a microprocessor coupled to the bus (not explicitly shown in the figure, but taught in col.2, lines 40-51, col.3, lines 22-24 as on-chip microprocessor);

c) memory [1] :

a plurality of functionalities ([3][4]). Comprising

1) interconnect (see the connection to [3] and [4]);

2)analog circuit ([4]);

3) a digital functional block to the interconnect (see fig.1[3]);

d) programmable I/O (see fig.1 [5], col.3, lines 18-19, see also col.2, lines 1-14 for background teaching of programmable logic blocks);

e) analog functional block [4] and digital functional block [4] (see fig.1, col.1, lines 15-19, see also col.2, lines 1-14 for background teaching of programmable logic blocks).

9. AS to claim 12, Insenser also included a moicrocontroller (see fig.1[2]).

10. As to claim 13, 14, Insenser also included user input (see the high level language ,HDL, in col.2, lines 27-39, see also col.5, lines 4-6).

11. As to claim 15, Insenser also included configuration state (see also col.2, lines 1-14 for background teaching of programmable configuring and reconfiguring features of logic blocks, see the configuration contexts in col.4, lines 1-7).

12. As to claim 16, see paragraph # 10 above.

13. As to claims 17,18,25, Insenser also taught at least one block of digital blocks being coupled to at least one analog circuit block (see any point of the digital blocks probed with the analog subsystem in col.3, lines 42-44); wherein the digital circuit block were coupled to the analog circuit blocks (see inside blocks in fig.1 [3][4]), and at

least one second digital block and analog block was coupled to microprocessor (see how the microprocessor read and write to analog and digital circuit blocks in col.3, lines 38-42, lines 45-47, see also how the lookup table mapped the functional blocks in col.4, lines 26-36, see also the inside functional blocks of analog subsystem [4] in col.4, lines 38-51).

14. As to claim 19, Insenser also included a plurality of analog functions (see the inside functional blocks of analog subsystem [4] in col.4, lines 38-51).

15. As to claim 20,21, Insenser did not explicitly show the third digital circuit block was coupled to the fourth analog block as claimed. However, since Insenser already taught any point of the digital circuit blocks could probed with the analog circuit (see col.3, .lines 41-44), and that the system let user build a custom made application out of these circuit blocks (se col.4, lines 45-51), the examiner believes that any particular order, or pair, of connection between the digital blocks and analog blocks was possible through the reconfugurable system, and furthermore, no particular advantage of the third digital block coupled to the fourth analog block is being reflected into the claim, therefore, it is viewed as any third digital block and any fourth analog digital block connection. Insenser did have the third digital circuit block (see any third inside blocks in fig.1 [3]), and a fourth analog block (see one of plurality of functional blocks in col.4, lines 38-46, see also the routing channels in col.3, lines 29-30, col.5, lines 5-11).

16. As to claim 22, see fig.1 [3][4]).

17. As to claim 26, Insenser's I/O also sent signals to microprocessor (see col.4, lines 52-53).

18. As to claim 27, Insenser also included plurality of I/O blocks with the digital and analog block (see the interconnection between the [7][8] and [3][4] in fig.1).

19. As to claim 28, Insenser also included a second I/O [8] connected to at least one analog blocks (see fig.1).

20. As to claim 29, see interconnection between digital blocks [3] and analog blocks [4].

21. As to claim 30, Insenser also include a connection between a third I/O [6] and the memory [1] (see fig.1).

22. As to claims 31,32, Insenser also included a plurality of registers and latches for storing programming data for the digital and analog circuit blocks (see the FF's in col.4, lines 21-36, see also fiug.2).

23. As to claim 35, Insenser disclosed :

a) a plurality of I/O circuit blocks (see figu.1 [5][6][7][8][10]);

b) a plurality of programmable analog circuit bocks (see the inside functional elements in fig.1 [4]);

c) a plurality of programmable digital circuit blocks (see the array of digital blocks in fig.1 [3]);

The plurality of I/O circuit blocks connected to the plurality of programmable analog circuit bocks the plurality of programmable digital circuit blocks (see interconnections in fig.1).

24. As to claim 36, Insenser's I/O also sent signals to at least a first one of the plurality of analog circuit blocks, and the analog sent to different one of the I/O blocks (see the communication connection between either [5][6][7][8] or [10] to [4] in fig.1).

25. As to claim 37, Insenser disclosed a plurality of programmable digital circuit blocks (see fig.1 [3]);

b) a plurality of analog circuit blocks (see fig.1 [4], see the plurality of analog functional blocks in col.4, lines 37-51).

c) a memory connected to the plurality of digital and analog circuit blocks (see fig.1).

26. Insenser did not explicitly show his analog and digital circuit blocks received first subset of programming data and second subset of programming data , respectively, as claimed. However, Insenser , in the same patent , disclosed a microprocessor was able to read the stored programming data (e.g. the two configuration contexts) for both the digital circuit and analog circuits (see col.2, lines 51-59). The source for storing the programming data (configuration contexts) was not clearly shown, but the examiner believes it had to be from the memory because the microprocessor had to be reading or writing into memory , therefore, since no other memory being presented by Insenser, the fist programming data (configuration) for the analog and second programming data (configuration) for the digital circuit had to be received from the memory based on the microprocessor command (see also col.4, lines 1-3).

27. As to claims 38-41, Insenser did not explicitly show the connections of the particular ones of the circuit blocks (e.g. the second one of the analog circuit block) as claimed. However, since Insenser already taught any point of the digital circuit blocks

could probed with the analog circuit (see col.3, .lines 41-44), and that the system let user build a custom made application out of these circuit blocks (se col.4, lines 45-51), the examiner believes that any particular order, or pair, of connection between the digital blocks and analog blocks was possible through the reconfugurable system (see also the routing channels in col.3, lines 29-30, col.5, lines 5-11).

28. As to claim 51, Insenser also included at least three digital blocks (see fig.1 [3]) connected in series and or parallel (see the row or column connections of three blocks in [3]), controlled by lookup table [LUT] including a cascade bit (see the LUT and cascade bits in col.4, lines 15-36) for determining the adjacent circuit blocks (see the 16 x 4 memory, the next bit position had to be an adjacent location or block, for example, 0001 is next to 0000 in the memory).

29. As to claim 52, Insenser disclosed :

a) a micro controller {see fig.1 [2));

b) a subsystem comprising a functionality[3][4] coupled to the microcontroller (see (fig.1 [3][4]);

c) coupling mechanism (see the reconfiguration tools in col.3, lines 45-612), wherein selectively, the functionality was configured to execute a first function according to a first input (see the configured programmable digital or analog cells), and implement a connection state (map, routing, placement) for the system by which the system was connectable to external entity [external devices] according to a second input [interface 7] (see col.3, lines 14-25).

30. As to claims 53,54,55, see the digital and analog functions in col.3, lines 14-20).

31. As to claim 56, Insenser also included first sub-functionality [digital function 3] and second sub-functionality [analog 4], wherein the interconnection mechanism was configured to interconnect the first sub-functionality [digital function 3] and second sub-functionality [analog 4] according to a user input of third type (see CAD tools for configuring the programmable cells in col.3, lines 45-61).

32. AS to claim 57, Insenser also included time bases according to user input (see the operating frequencies in col.4, lines 40-44, it was user input because it was programmable).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claim 2, 9,10,23,24,33,34,42-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre (6,460,172) in view of Furtek et al. (5,894,565).

34. As to claim 2, Insenser did not specifically show the circuit was selected from a group of microcontrollers and other integrated circuits as claimed. However, Furtek

disclosed a selected group of microcontrollers [DFE] and other integrated circuits [programmable circuit cell 11] (see figs.12 , col.5, lines 3-29, col.11, lines 56-65 for the DFE 83 as microcontrollers and each of the partitions of programmable logic cells 11). It would have been obvious to one of ordinary skill in the art to use Furtek in Insenser for including the selected circuit block as claimed because the use of Furtek could provide Insenser the processing capability to adapt to additional circuit blocks , and thereby expanding the processing structure of the system, and because Insenser also taught an interface [8] to communicate with other circuit block [FIPSOC], and it should be reasonable to presume to have the same structure of the current circuit block, FIPSOC which had microcontroller and other integrated circuits in a group, and therefore, a selected group of microcontrollers and integrated circuits was possible, and in doing so, provided a motivation. Insenser is used as primary reference because it taught clearly the microprocessor being used with analog and digital blocks. Furtek is used as a secondary reference because it showed groups of microcontrollers and integrated circuits was implemented.

35. AS to claims 9,10,23,24, although Insenser disclosed a RAM [1], it did not show a read only memory (claim 9) or erasable memory (claim 23) as claimed. However Furtek disclosed a erasable read only memory [EPROM, electrically erasable programmable rom] in a logic circuit cell (see col.1, lines 20-28). It would have been obvious to one of ordinary skill in the art to use Furtek in Insenser for including the read only memory as claimed because the use of Furtek could provide Insenser a greater storage capability to adapt to specific access format of a given type of memory, such as

the read only, and because Furtek already taught the read only memory being used in programmable integrated logic circuit blocks, one of ordinary skill in the art should be able to recognize the advantages of adding read only memory into Insenser's circuit block for the expanded storage structure compatibility, and for the above reason, provided a motivation.

36. As to claims 33,34, Insenser did not specifically show the global or macro routing matrix for coupling the subsets or plurality of analog and digital blocks as claimed. However, Furtek disclosed a global and macro routing matrix for coupling subsets of digital and analog blocks (see the routing of the signals in the partitioning of the matrix cells in col.5, lines 10-22, see also the logic circuit cells intersections with the function elements 83 as digital and analog circuit blocks in col.11, lines 60-66) . It would have been obvious to one of ordinary skill in the art to use Furtek in Insenser for including the global or macro routing matrix as claimed because the use of Furtek could extend the processing structure of Insenser to accept additional macro blocks of the circuit, and because Insenser did disclose a large granularity of programmable cells (see col.4, lines 15-21), which was an indication of the need of a global or macro routing matrix into the system in order to manage great number circuit blocks in macro or global level, and in doing so, provided a motivation.

37. As to the mathematical functions in the digital circuit blocks in claims 42, 44, since Insenser already taught his digital and analog circuit hardware was used for measuring the dimension, weight, and calculating the acceleration, and accounting

credit (e.g. see col.6, lines 6-18), Insenser's digital circuit must have mathematical functions.

38. As to claims 43,45, see plurality of analog functions in col.4, lines 37-43).

39. As to claim 46, Furtek's routing matrix also included the connection of the second subset often analog and digital circuit blocks (see the second matrix partitions in col.5, lines 4-22, se also the digital and analog cells in col.11, lines 60-67).

40. As to claim 47, Furtek also included M x N macros (see the matrix 4 x 4 in col.5, lines 2-18, see also the analog circuit cells in col.11, lines 60-67, se also fig.12).

41. As to claim 48, see the analog and comparator functions in col.11, lines 60-67 in Furtek, see also the analog functions in col.4, lines 37-51 in Insenser).

42. As to claim 49, Insenser's digital blocks were connected in series (see fig.1[first row 3]).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

43. Claim 50 is rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Furtek (5,894,565).

44. As to claim 50, Furtek disclosed a programmable analog circuit (see fig,12, each block could be an analog block), comprising n x m plurality of analog circuits blocks

(see the analog logic blocks in col.11, lines 60-67), each coupled to adjacent block configured to provide analog functions.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

45. Claims 58,59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser (6,460,172) in view of Gammal et al. (5,754,826).

Insenser disclosed :

a) microcontroller (see fig.1 [2], col.3, lines 14-25);

b) a subsystem coupled to the microcontroller comprising a plurality of analog functions and digital functions that were both configured by user input [CAD] (see fig.1, col.3, lines 37-61);

c) an interconnection (see the routing channels, interaction) configurable for selectively interconnecting the plurality of analog and digital functions according to user input (see fig.1, see the reconfigurable programmable cells in col.3, lines 45-61, see the programmable analog cells and digital cells in col.3, lines 14-24);

d) a coupling mechanism coupled to the subsystem that was configurable to implement connection state for system by which the system was connectable to external entity according to user input (see the external interface [8] in fig.1);

e) selecting the functions and the interconnection state (see the reconfigurable programmable cells by the CAD tools in col.3, lines 45-61, see the routing and placement for the interconnection state);

f) selecting the connection state [configuration] to effectuate a connection between the system and external entity correspond to a function (see either external interface 7 or 8 infig.1, see also col.4, lines 61-65 for example of PC connection).

46. Although Insenser showed a plurality of analog and digital and mixed functions (see fig.1 [3][4], see mixed signal for mixed digital and analog functions in col.3, lines 55-56), it did not specifically show a list of the analog and digital functions exactly as claimed. However, Gammal disclosed a netlist (see fig.3) including a plurality of functional cells (see the netlist for the symbolic representation in col.2, lines 17-26 for background, see col.6, lines 17-38 for the selected macro cells in the list). It would have been obvious to one of ordinary skill in the art to use Gammal in Insenser for including the list of he functionalities as claimed because the use of Gammal could provide Insenser the ability to control the plurality of the functional cells in a predetermined set of program sequence, such as a netlist, thereby enhancing the connectivity of functional cells in a given format in the system , and because Insenser also taught the mapping and the library functions of the programmable cells which was an indication of the applicability of a list of the functional cells in the system in order to provide the enhanced programmable scheme , and in doing so, provided a motivation. Insenser is used as primary reference because it showed clearly the interconnection a microcontroller with the analog and digital functional cells. Gammal is used as

secondary reference because it showed clearly the particular use of the functional cell netlist .

47. As to claim 58, Insenser also included a plurality of time bases (see the operating frequency of the filters in col.4, lines 41-44).

48. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Naglestad et al. (5,481,471) is cited for the basic teaching of selection of the plurality of digital and analog functions (see fig.1, se the selected functional blocks in col.3, lines 24-54);

b) Ting (5,457,410) is cited for the matrix routing of the circuit blocks (e.g. see col.4, lines 5-55).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

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21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP